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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,851	12/20/2001	Claude Thibeault	17273-6US-AD	1516

20988 7590 05/12/2010

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EXAMINER	
GHULAMALI, QUTBUDDIN	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
05/12/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/022,851	THIBEAULT ET AL.	
	Examiner	Art Unit	
	Qutbuddin Ghulamali	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to amendment filed 9/9/2009.

2.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Balakrishnan et al (USP 5,101,347) in view of Tan et al (USP 5,815,031) and further in view of Hamamoto et al (IEEE paper).

Regarding claims 1, 18 and 21, Balakrishnan discloses a data transmitter and receiver configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals, (for example, to implement the transmission of a 32-bit data character, i.e. doubleword data, each of four 8-bit wide transmitter FIFO chips provides a data path for transferring byte-wide data slices through four associated bus driver chips to the data bus for capture by a similarly configured receiver arrangement, col. 1, lines 35-44) each of the first and second output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of a plurality of conductive paths, said data transmitter comprising:

wherein a time between a state transition on an input signal and the corresponding state transition on the corresponding output signal exceeds a time between a state transition on an input signal of another set and the corresponding state transition on the corresponding output signal by a delay period T DLY, and

wherein the period T CLK is greater than the delay period T DLY (col. 2, lines 10-39). Balakrishnan, however, does not explicitly disclose, "adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries an output signal of another set". Tan in a similar field of endeavor discloses an improved signal routing scheme includes a plurality of dynamic signal lines disposed in parallel to each other wherein adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries an output signal of another set (col. 2, lines 32-44, 53-60). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use plurality of dynamic signal lines parallel to each other (adjacent conductive paths) separated by conductive path to carry output signal of another set as taught by Tan in the system of Balakrishnan because it can mitigate crosstalk noise by reducing unwanted coupling between signal paths. Balakrishnan and Tan combined does not disclose,

a plurality of first latches, each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions, with consecutive first transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being

further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition; and

a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition. However, Hamamoto et al discloses a plurality of first latches (fig. 4, F and B latches), each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions (tin (rise and fall), with consecutive first transitions being separated by a time period T_CLK (f-CLK and B-CLK), (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition (page 771, section B; page 772, first column and second column); and a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input

signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition (fig. 4; page 771, section B; page 772, first column and second column). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the teachings of Mamamoto in the combined system of Balakrishnan and Tan because it can multibank operation of transmission line with minimal skew allowing transfer of data at a higher speed.

Regarding claims 13, Balakrishnan discloses data transmitter and the plurality of conductive paths are fabricated on the same semiconductor substrate (col. 4, lines 13-18).

Regarding claim 14, the limitation data transmitter is further configured and arranged to receive an operating voltage from two power rails, and wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths is well known, power and ground return lines are separation is a common occurrence in design practice to provide communication and transfer of signals with minimum crosstalk and noise coupling by separating the power lines or planes such as top and bottom of circuit boards and therefore an obvious choice to a person of ordinary skill in the art to utilize the common knowledge available in the design circle.

Regarding claim 15, Balakrishnan discloses each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission

lines, and wherein the data transmitter is further configured and arranged to couple the first clock signal to one of the plurality of parallel transmission lines (col. 3, lines 13-55).

Regarding claim 16 Balakrishnan and Tan combined disclose substantially all limitations of the claim above, except does not disclose a plurality of buffer coupled to a different one of the latch outputs of the first and second latches. However, Hamamoto in a similar field of endeavor discloses a number of buffers arranged to provide bufferto each of the plurality of latches (fig. 4). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the teachings of Hamamoto to provide buffers to each of the plurality of latches in the combined system of Balakrishnan and Tan because it can allow proper detection of rise and fall edges minimize skew conditions.

Regarding claim 17, Balakrishnan discloses data transmitter further comprising a delay element configured and arranged to receive the first clock signal and to produce the second clock signal, wherein the second clock signal is delayed with respect to the first clock signal by the delay period T_DLY (col. 2, lies 10-39, fig. 2).

Regarding claim 19, Balakrishnan discloses wherein the second clock signal is substantially identical to the first clock signal (fig. 3).

Regarding claim 20, Balakrishnan discloses the delay period T_DLY is at least as long as a rise time of the data clock signal (col. 2, lines 10-39).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutbuddin Ghulamali whose telephone number is (571)-

272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG.
May 8, 2010.

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611